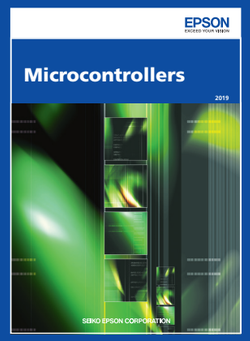
EPSON
EXCEED YOUR VISION



America

Epson America, Inc.
Headquarter:
3840 Kilroy Airport Way
Long Beach, California 90806-2452 USA
Phone: +1-562-290-4677

San Jose Office:
214 Devcon Drive
San Jose, CA 95112 USA
Phone: +1-800-228-3964 or +1-408-922-0200

Europe

Epson Europe Electronics GmbH
Riesstrasse 15, 80992 Munich, Germany
Phone: +49-89-14005-0 FAX: +49-89-14005-110

Asia

Epson (China) Co., Ltd.
4th, Floor, Tower 1 of China Central Place, 81 Jianguo Road, Chaoyang District, Beijing 100025 China
Phone: +86-10-8522-1199 FAX: +86-10-8522-1120

Shanghai Branch
Room 1701 & 1704, 17 Floor, Greenland Center II,
562 Dong An Road, Xu Hui District, Shanghai, China
Phone: +86-21-5330-4888 FAX: +86-21-5423-4677

Shenzhen Branch
Room 804-805, 8 Floor, Tower 2, Ali Center, No.3331
Keyuan South RD(Shenzhen bay), Nanshan District, Shenzhen 518054, China
Phone: +86-10-3299-0588 FAX: +86-10-3299-0560

Epson Taiwan Technology & Trading Ltd.
15F., No.100, Songren Rd., Sinyi Dist., Taipei City 110. Taiwan
Phone: +886-2-8786-6688

Epson Singapore Pte., Ltd.
1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

Seiko Epson Corp.
Korea Office
19F, KLI 63 Bldg., 60 Yoido-dong, Youngdeungpo-Ku, Seoul 150-763, Korea
Phone: +82-2-784-6027 FAX: +82-2-767-3677

Seiko Epson Corp.
Sales & Marketing Division

Device Sales & Marketing Department
421-8, Hino, Hino-shi, Tokyo 191-8501, Japan
Phone: +81-42-587-5816 FAX: +81-42-587-5116

Epson semiconductor website global.epson.com/products_and_drivers/semicon/

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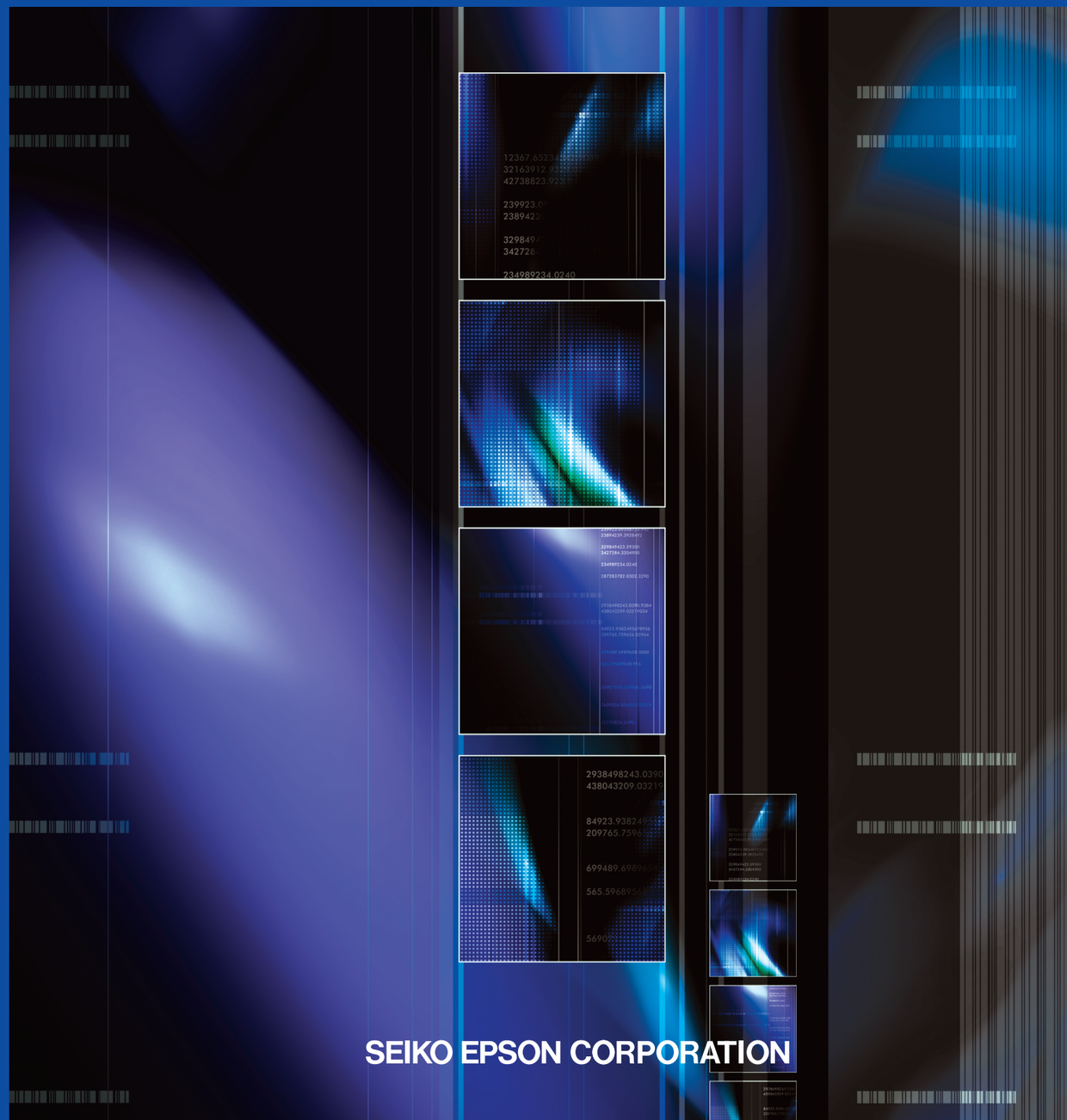
ASICs

Gate Arrays / Embedded Arrays / Standard Cells

2019



SEIKO EPSON CORPORATION

Business Concept

Expanding use of smartphones and tablets is giving broadband internet and wireless communications even greater roles in our daily lives, and making the arrival of the ubiquitous network society an inevitable reality. In particular, semiconductors for use in portable devices, information terminals, in-vehicle devices and FA devices are expected to provide higher performance in terms of thinner structure, lighter weight, and longer operation with limited power supply. We have been focusing on the creation of compact, low-power semiconductors since we started the development of CMOS LSI for watches in 1969. Since then, we have steadily built up our expertise in energy-saving, space-saving, and time-saving designs. This has enabled us to quickly obtain the semiconductor development technology needed to meet the demands of the new era of ubiquitous networks. Our concept is to develop "saving technologies" to reduce power consumption, development times, and implementation space. Our goal is to be a true partner for you, providing you with strategic advantages, enhancing your customer value based on our "saving technologies" and mixed analog/digital technologies that we have cultivated, as well as our design capabilities, manufacturing capabilities and stable supply that can satisfy your detailed requirements.

Environmental Responsibility

Epson semiconductor technology provides environmental value to customers by creating and manufacturing eco-friendly products.

1) We Epson's products are surely complying with the Eu-RoHS (2011/65/EU) Directive.
2) We are releasing information about the containing chemical substances of products at web-site.
   Product of QFP & BGA are described in the following URL.
   global.epson.com/products_and_drivers/semicon/information/package_lineup.html *Some products are excluded.

Environmental management system third party certification status
ISO14001
Type of certification : ISO 14001: 2015, JIS Q 14001: 2015
Awarded to : TOHOKU EPSON CORPORATION, SEIKO EPSON CORPORATION
(Fujimi Plant, Suwa Minami Plant)
Certified by : Bureau Veritas Japan Co., Ltd.
Date of certification : April 3, 1999

Type of certification : ISO 14001: 2015
Awarded to : Singapore Epson Industrial Pte. Ltd.
Certified by : SGS
Date of certification : Jan 12, 1999

Epson's Quality Policy

Keeping the customer in mind at all times, we make the quality of our products and services our highest priority. From the quality-assurance efforts of each employee to the quality of our company as a whole, we devote ourselves to creating products and services that please our customers and earn their trust.
Epson has acquired ISO9001 and IATF16949 certification with its IC, module and their application products.

Quality Management system third party certification status
ISO9001
Type of Certification : ISO9001: 2015 , JIS Q 9001: 2015
Awarded to : TOHOKU EPSON CORPORATION, SEIKO EPSON CORPORATION
(Fujimi Plant, Suwa Minami Plant, Hino Office)
Certified by : Bureau Veritas Japan Co., Ltd.
Certificate No. : 3762381
Initial Date of Certification : October 10, 1993

Type of Certification : ISO9001: 2015
Awarded to : Singapore Epson Industrial Pte. Ltd.
Certified by : SGS
Certificate No. : SG03/00011
Initial Date of Certification : February 4, 2003

IATF16949
Type of Certification : IATF16949:2016
Awarded to : TOHOKU EPSON CORPORATION, SEIKO EPSON CORPORATION
(Fujimi Plant, Suwa Minami Plant, Hino Office), EPSON EUROPE ELECTRONICS GmbH
Certified by : Bureau Veritas Japan Co., Ltd.
Certificate No. : 281371
Initial Date of Certification : Dec 9, 2017

Type of Certification : IATF16949:2016
Awarded to : Singapore Epson Industrial Pte. Ltd.
Certified by : SGS
Certificate No. : SG07/00021
Initial Date of Certification : May 2, 2018

ASICs

Product number explanation

●Device

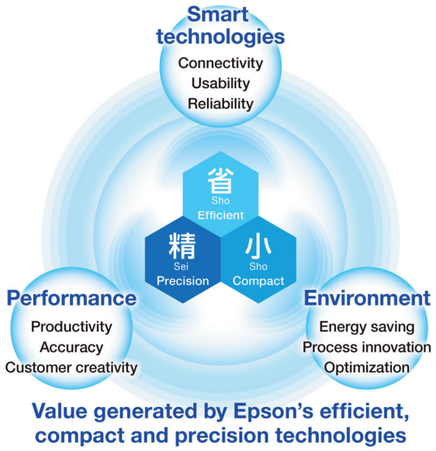
S1L60173F00A000

- Packing specification
- Specifications
- Shape (B : BGA, WCSP, F : PlasticQFP)
- Model number
- Model name (K : Stadard Cells, L : Gate Arrays, X : Embedded Arrays)
- Product classification (S1/S2/S7 : Semiconductor)

C O N T E N T S

History of Epson semiconductor

Value Generated by Epson Technologies



Value generated by Epson's efficient, compact and precision technologies

Smart technologies

Create convenient and easy-to-use products that can be used anytime and anywhere, and which help customers reduce waste, and save effort, time and money.

Environment

Leverage Epson products to reduce environmental impact by improving customers' work processes, and contribute to a sustainable society.

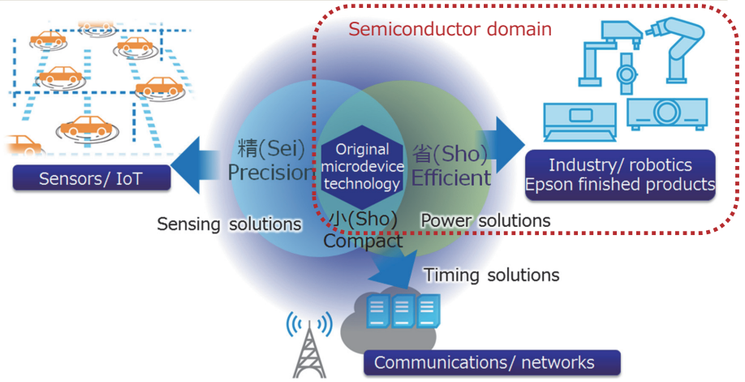
Performance

Use outstanding products to contribute to customers' performance through productivity, accuracy and creativity.

The role of Microdevices Div. and Semiconductor domain

Microdevices Vision and Strategy: Supporting the Four Innovations

Contribute to Epson's finished products and to the development of smart communications, power, transportation and manufacturing systems with advanced Epson quartz timing and sensing solutions and low-power semiconductor solutions.



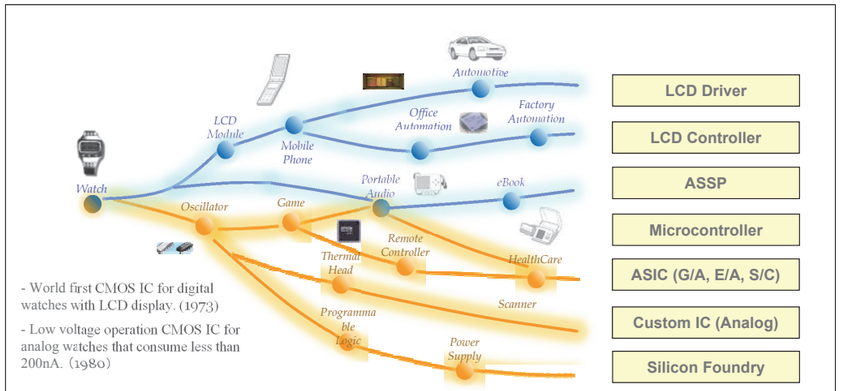
Semiconductor business contribute to the value creation of the Epson finished product, by advanced "Power Saving" solutions.

History of Epson semiconductor

ASICs

History of Epson Semiconductor's Technology

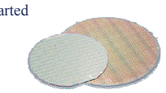
As the semiconductor division of "worldwide watch maker Seiko", semiconductor business has expanded into LCD Drivers, ASICs and MCUs from IC for Watches. These businesses are all based on Epson's energy-saving technology.



Energy-Saving Technology ; Technology that reduces power consumption from both sides of process and circuit have been nurtured by Epson over 40 years since division was founded.

Epson Semiconductor's History

●	1969	Development of CMOS IC for watches started
○	1973	CMOS IC production started in Headquarter
●	1980	Fujimi plant (B-wing, 4 inch) operation started
○	1984	A-wing (5 inch) operation started
○	1985	D-wing (6 inch) operation started
●	1991	Sakata plant (S-wing,6 inch) operation started
○	1993	ISO9000 series certified
○	1994	Singapore assembly plant (SEP) operation started
●	1997	T-wing (8 inch, Sakata) operation started
		ISO14001 certified
○	2001	T-wing manufacturing line expanded
○	2006	ISO/TS16949 certified
●	2010	Microdevices Operations Division started



ASIC Product Lineup

Epson's ASIC offerings aim to provide the best overall solution thus enabling our customers to get products to market successfully. Epson ASIC products include gate arrays that address the need for fast turnaround, at low IC development costs; Standard Cells, that make system solutions possible at the lowest unit price, and embedded arrays that combine the fast turnaround time of gate arrays with the ability to implement system level functionality on chips available with standard cells.

Epson ASIC

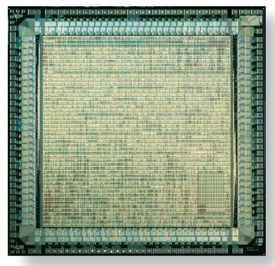
- Abundant supporting achievements ever since 1982
- Entire operation of design and manufacture in our own factory
- ISO9001 & IATF16949 certificated

Gate Arrays

S1L60000	0.25μm	Core 1.8V, 2.0V, 2.5V
S1L50000	0.35μm	Core 2.0V, 2.5V, 3.3V 5V interface
S1L5V000	0.35μm	Core 3.3V, 5.0V 5V single power supply

The gate array is a member of the ASIC family that offers quick turnaround time during the development cycle at the lowest development cost. This is achieved by Epson stocking pre-fabricating Base/Bulk wafers that have transistors arranged in the form of an array. Our customers design the "wiring", that connects the transistors, that bring specific functionality to the design of the ASICs.

Base arrays are prefabricated with different numbers of transistors giving customers a wide range of choices to implement their circuits. This offers flexibility to customers by giving them the choice of adding or subtracting functionality from the design.



ASIC Product Lineup

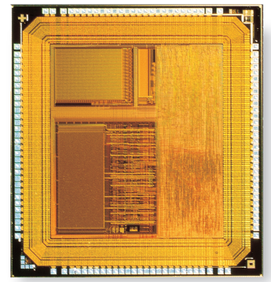
ASICs

Embedded Arrays

S1X80000	0.15μm	Core 1.8V 3.3V single power supply with LDO
S1X60000	0.25μm	Core 1.8V, 2.0V, 2.5V 5V interface
S1X50000	0.35μm	Core 2.0V, 2.5V, 3.3V 5V interface
S1X5V000	0.35μm	Core 3.3V, 5.0V 5V single power supply

The embedded array combines the fast turnaround time of gate arrays with the ability to implement system level functionality available in standard cells. The fast turnaround is accomplished by starting some of the wafer fabrication processes in parallel with the embedded array design process. In selecting an embedded array approach, the designer trades off the ability to change the base array in the last minute, possible with a gate array, with the need to implement system level functionality, with gate array like turnaround.

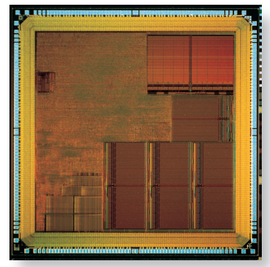
By offering gate arrays, standard cells, and embedded arrays; Epson offers a choice to meet the individual needs of our customers.



Standard Cells

S1K80000	0.15μm	Core 1.8V 3.3V single power supply with LDO
S1K60000	0.25μm	Core 1.8V, 2.0V, 2.5V 5V interface

Standard cells (cell-based ASICs) are semi-custom ICs that enable optimally designed internal logic cells, memories such as ROM and RAM, CPU, and analog circuits to be implemented all on the same chip. As such, standard cells enable more design flexibility than gate arrays, offer more advanced functionality and higher integration, and can be developed as system LSI optimized for the customer's needs. Such optimization enables the achieving of ever more advanced functionality and lower power consumption.



Gate Arrays

Epson's Gate Array is a suitable solution for replacing existing devices because this Gate Array option gives flexibility to adapt the power supply and layouts of other various signals. Furthermore Epson has invested on the new Gate Array series called "S1L5V000" which supports 5V single power supply with 0.35μm process. Since it is a new series, it is also suitable for long life time applications.

S1L50000 Series

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V
3.3V	3.3V
	5.0V

Series		S1L50000 Series													
Features		• Ultra large scale integration (0.35 μm CMOS, using 2-, 3- or 4-layer interconnect process) • High-speed operation (0.14 ns delay at 3.3 V, with 2-input power NAND Typ.) • Low power consumption (Internal cell: 0.7μW/MHz/gate at 3.3 V) • Drivability (I_{OL} = 0.1, 1, 3, 8, 12, 24 mA, PCI at 5.0 V, I_{OL} = 0.1, 1, 2, 6, 12 mA, PCI at 3.3 V, I_{OL} = 0.1, 0.5, 1, 3, 6 mA at 2.5 V, I_{OL} = 0.05, 0.3, 0.6, 2, 4 mA at 2.0 V)													
Model	Double layer	S1L50062	S1L50122	S1L50282	S1L50552	S1L50752	S1L50992	S1L51252	S1L51772	S1L52502	S1L53352	S1L54422	S1L55062	S1L56682	S1L58152
	Triple layer	S1L50063	S1L50123	S1L50283	S1L50553	S1L50753	S1L50993	S1L51253	S1L51773	S1L52503	S1L53353	S1L54423	S1L55063	S1L56683	S1L58153
	Quadruple layer	S1L50064	S1L50124	S1L50284	S1L50554	S1L50754	S1L50994	S1L51254	S1L51774	S1L52504	S1L53354	S1L54424	S1L55064	S1L56684	S1L58154
Total BC (Row gates)		5.8k	12.0k	28.8k	55.5k	75.8k	99.2k	125.8k	177.1k	250.2k	335.9k	442.2k	506.7k	668.6k	815.5k
Usable gates	Double layer	2.9k	6.0k	14.4k	26.1k	35.7k	46.7k	56.6k	79.7k	112.6k	144.5k	176.9k	202.7k	267.5k	326.2k
	Triple layer	5.1k	10.6k	25.3k	47.2k	64.4k	84.4k	100.7k	132.8k	187.7k	251.9k	309.5k	354.7k	468.0k	570.9k
	Quadruple layer	5.5k	11.4k	27.3k	52.8k	72.0k	94.3k	119.5k	168.2k	237.7k	319.1k	397.9k	456.1k	601.7k	734.0k
Total Lead Count	80μm	—	56	88	124	144	168	188	224	264	308	352	376	432	480
	70μm	48	64	104	144	168	192	216	—	—	—	—	—	—	—
Delay Time	Internal gates	t_{pd} = 0.14 ns (3.3 V, F/O 2, typical wire load), 0.21 ns (2.0 V, F/O 2, typical wire load)													
	Input buffer	t_{pd} = 0.38 ns (5.0 V, F/O 2, typical wire load) Level shifter: 0.4 ns (3.3 V, F/O 2, typical wire load), 1.3 ns (2.0 V, F/O 2, typical wire load)													
	Output buffer	t_{pd} = 2.12 ns (5.0 V) Level shifter: 2.02 ns (3.3 V), 3.9 ns (2.0 V) CL = 15 pF													
I/O level		CMOS, LVTTL, PCI-5V, PCI-3.3V													
Input modes		LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail-safe, Gated													
Output modes		Normal, Open drain, 3-state, Bidirectional, Fail-safe, Gated													

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

S1L5V000 Series

Core	I/O
5.0V	5.0V
3.3V	3.3V

Series		S1L5V000 series							
Features		• Large scale integration (0.35 μm CMOS, using 2-, 3-, 4-layer interconnect process) • High speed operation (internal gate delay: 0.19ns at 5V, 0.29ns at 3.3V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 5V 1.3μW/MHz/BC, 3.3V 0.54uW/MHz/BC) • Drive capacity (I_{OL}=0.1, 1, 3, 8, 12, 24mA at 5.0V, I_{OL}=0.1, 1, 2, 6, 10mA at 3.3V)							
Model	Double layer	S1L5V012	S1L5V042	—	S1L5V112	—	S1L5V252	—	S1L5V482
	Triple layer	S1L5V013	S1L5V043	S1X5V513*	S1L5V113	S1X5V523*	S1L5V253	S1X5V533*	S1L5V483
	Quadruple layer	S1L5V014	S1L5V044	S1X5V514*	S1L5V114	S1X5V524*	S1L5V254	S1X5V534*	S1L5V484
Total BC (Row gates)		8.8k	42.0k	26.0k	109.2k	90.3k	254.3k	235.0k	479.9k
Usable gates	Double layer	2.6k	12.6k	—	32.7k	—	63.5k	—	119.9k
	Triple layer	5.3k	25.2k	14.3k	65.5k	49.7k	139.8k	129.3k	239.9k
	Quadruple layer	6.1k	29.4k	16.9k	76.4k	58.7k	165.3k	152.8k	287.9k
Total Lead Count		48	104		168		256		308
Delay Time	Internal Gates	t_{pd}=0.19ns (5.0V operation, F/O=2, typical wiring load), t_{pd}=0.29ns (3.3V operation, F/O=2, typical wiring load)							
	Input Buffer	t_{pd}=0.45ns (5.0V operation, F/O=2, typical wiring load), t_{pd}=0.55ns (3.3V operation, F/O=2, typical wiring load)							
	Output Buffer	t_{pd}=2.07ns (5.0V operation, CL=15pF), t_{pd}=2.95ns(3.3V operation, CL=15pF)							
I/O level		CMOS, TTL, LVTTL							
Input modes		TTL, LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail-safe, Gated							
Output modes		Normal, Open-drain, 3-state, Bidirectional, Fail safe, Gated							

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

*: Analog PLL built in master

S1L60000 Series

Core	I/O
1.8V	1.8V
	3.3V
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V

Series		S1L60000 Series									
Features		• Ultra large scale integration (0.25 μm CMOS, using 3-, 4-layer interconnect process) • High-speed operation (107 ps internal gate delay at 2.5 V, with 2-input NAND Typ.) • Low power consumption (Internal cell: 0.18μW/MHz/gate at 2.5 V, with 2-input NAND Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24 mA at 3.3 V, I_{OL} = 0.1, 1, 3, 6, 9,18 mA at 2.5 V, I_{OL} = 0.05, 0.3, 1, 2, 3, 6 mA at 2.0 V, I_{OL} = 0.045, 0.27, 0.9, 1.8, 2.7, 5.4 mA at 1.8 V)									
Model	Triple layer	S1L60093	S1L60173	S1L60283	S1L60403	S1L60593	S1L60833	S1L61233	S1L61583	S1L61903	S1L62513
	Quadruple layer	S1L60094	S1L60174	S1L60284	S1L60404	S1L60594	S1L60834	S1L61234	S1L61584	S1L61904	S1L62514
Total BC (Row gates)		99.2k	171.8k	284.4k	400.3k	595.4k	831.6k	1,234.9k	1,587.8k	1,903.0k	2,519.6k
Usable gates	Triple layer	59.6k	103.1k	142.2k	200.2k	297.7k	332.7k	494.0k	635.1k	761.2k	1,007.9k
	Quadruple layer	69.5k	120.2k	184.9k	260.2k	387.0k	415.8k	617.5k	793.9k	951.5k	1,259.8k
Total Lead Count	80μm	—	—	—	—	—	284	344	388	424	488
	70μm	112	148	188	224	272	—	—	—	—	—
Delay Time	Internal gates	t_{pd} = 107 ps (2.5 V, F/O 1, typical wire load)									
	Input buffer	t_{pd} = 270 ps (2.5 V, F/O 2, typical wire load)									
	Output buffer	t_{pd} = 1600 ps (2.5 V, CL = 15 pF)									
I/O levels		CMOS, LVTTL, PCI-3.3V									
Input modes		CMOS, LVTTL, Pull-up/Pull-down, Schmitt, Level shifter, Fail-safe, Gated									
Output modes		Normal, Open drain, 3-state, Bidirectional, Level shifter, Fail-safe, Gated									

Note: Figures shown for usable gates are approximations. The actual number of usable gates varies according to the implemented circuitry.

Embedded Arrays

Creating hard macros for cells that are highly integrated and have advanced functionality enables development of system-on-a-chip designs, and utilization of the sea-of-gates structure in the logic means that the development period subsequent to the interconnection process is roughly equivalent to that for gate array chips.
In addition, the base array for LSI can be reused allowing only the logic block to be modified in development lead time equivalent to that for gate array chips.
Embedded array technology also facilitates circuit design changes and thereby helps avoid the risks associated with product modifications.

S1X5V000 Series

Series	S1X5V000 Series
Features	• High-density integration (0.35 μm CMOS process technology and 2/3/4-layer interconnect process) • High-speed operation (Internal gate delay: 0.19ns ps/5.0 V, 0.29ns/3.3 V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 1.3 μW/MHz/gate, 5.0V, 0.54 μW/MHz/gate, 3.3V, 2-input NAND Typ.) • Drivability (I_{OL}=0.1, 1, 3, 8, 12 mA at 5.0 V, 0.1, 1, 2, 6, 10 mA at 3.3 V

Core	I/O
3.3V	3.3V
5.0V	5.0V

S1X50000 Series

Series	S1X50000 Series
Features	• High-density integration (0.35 μm CMOS process technology and 3/4-layer interconnect process) • High-speed operation (Internal gate delay: 150 ps/3.3 V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 0.37 μW/MHz/gate, 3.3V, Typ.) • Drivability (I_{OL}=0.1, 1, 3, 8, 12, 24 mA at 5.0 V, I_{OL}=0.1, 1, 2, 6, 12 mA at 3.3 V, I_{OL}=0.1, 0.5, 1, 3, 6 mA at 2.5 V, I_{OL}=0.05, 0.3, 0.6, 2, 4 mA at 2.0 V)

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V
3.3V	3.3V
	5.0V

S1X60000 Series

Series	S1X60000 Series
Features	• High-density integration (0.25 μm CMOS process technology and 3/4/5-layer interconnect process, number of raw gates: 2,500,000 Max.) • High-speed operation (Internal gate delay: 107 ps/2.5 V, 2-input power NAND Typ.) • Low power consumption (Internal cell: 0.18 μW/MHz/gate, 2.5V, Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24 mA at 3.3 V, I_{OL} = 0.1, 1, 3, 6, 12, 24 mA at 2.5 V, I_{OL} = 0.05, 0.3, 1, 2, 4, 8 mA at 2.0 V)

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V

S1X80000 Series

Series	S1X80000 Series
Features	• Based on 0.15 μm CMOS process technology using 4/5-layer interconnect process • Internal gate delay: 47.1ps/1.8V, 2-input NAND Typ. • Lower power consumption (Internal cell: 0.063 μW /MHz/gate 2-input NAND Typ.) • Drive performance (I_{OL}=2,4,8,12mA at 3.3V)

Core	I/O
1.8V	3.3V
LDO	3.3V

Standard Cells

Standard cells (cell-based ASICs) are semi-custom ICs that enable optimally designed internal logic cells, memories such as ROM and RAM, CPU peripherals, and analog circuits to be implemented all on the same chip. As such, standard cells enable more design flexibility than do gate arrays, offer more advanced functionality and higher integration, and can be developed as a system-on-a-chip optimized for the customer's needs.
Such optimization leads to ever more compact, power-conserving devices.

S1K60000 Series

Series	S1K60000 Series
Features	• Ultra large scale integration (0.25 μm CMOS, using 3-, 4- or 5-layer interconnect process, number of raw gates: 3,900,000 Max.) • High-speed operation (Internal gate delay: 106ps/2.5V, 2-input NAND Typ.) • Low power consumption (Internal cell: 0.09 μW/MHz/gate, 2.5V, Typ.) • Drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24 mA at 3.3 V, I_{OL} = 0.1, 1, 3, 6, 9, 18 mA at 2.5 V, I_{OL} = 0.05, 0.3, 1, 2, 3, 6 mA at 2.0 V)

Core	I/O
2.0V	2.0V
	3.3V
2.5V	2.5V
	3.3V

S1K80000 Series

Series	S1K80000 Series
Features	• Based on 0.15 μm CMOS process technology using 4/5-layer interconnect process • Internal gate delay: 43.9ps/1.8V, 2-input NAND Typ. • Lower power consumption (Internal cell: 0.039 μW /MHz/gate 2-input NAND Typ.) • Drive performance (I_{OL}=2,4,8,12mA at 3.3V)

Core	I/O
1.8V	3.3V
LDO	3.3V

1. Flash

Series	S1X50000		S1X60000/S1K60000*
Operating Voltage	2.7 to 3.6V		2.3 to 2.7V
Memory Size	64K,128K,256K,512K,1M,2M-bit	256K,512K,1M,2M,4M-bit	256K,512K,1M,2M,4M-bit
I/O	8,16-bit		16-bit
Sector Size	1Kbyte/sector	4Kbyte/sector	4Kbyte/sector
Read Access Time (Max.)	50ns		50ns
Operating Current (Max.)	20mA		20mA
Standby Current (Max.)	10μA		10μA
Endurance Time (Max.)	1000 cycles		1000 cycles
Data Retention (Min.)	10years		10years
Temperature Range	0 to 70 ℃		0 to 70 ℃
Layer	3		3

* This macro cell uses the SuperFlash® technologies under license from SST UK Ltd.

2. PLL

Series	S1X5V000	S1X50000	
Macro Type	A35M	A35K	A35M
Operation Voltage	5.0V	3.0 to 3.6V	
Input Frequency	5MHz to 40MHz	32kHz	5MHz to 40MHz
Multiplication Ratio	x2 to x26	x610 to x4096	x2 to x26
Output Frequency	20MHz to 135MHz	20MHz to 135MHz	
Period Jitter	±2%	±3%	±2%
Duty	50%±10%	50%±10%	
Lock Up Time	100μs	100msec	100μs
Low Pass Filter	On chip	On chip	
Temperature Range	-40 to 110℃	-40 to 85℃	
Layer	3	3	

Series	S1X60000/S1K60000		S1X80000/S1K80000
Macro Type	A25K	A25M	A15M
Operation Voltage	2.3 to 2.7V		1.65 to 1.95V
Input Frequency	32kHz	5MHz to 150MHz	5MHz to 150MHz
Multiplication Ratio	Max. 16000	x1 to x16	x1 to x16
Output Frequency	20MHz to 200MHz		20MHz to 200MHz
Period Jitter	±2%	±200ps	POUT<=100MHz ±2% POUT>100MHz ±200ps
Duty	50%±5%		50%±5%
Lock Up Time	100msec	100μs	200μs
Low Pass Filter	On chip		On chip
Temperature Range	-40 to 85℃		-40 to 85℃
Layer	3		3

3. SRAM

Series	S1X5V000	
Macro Type	Standard	
Port	1-port	2-port (1R+1W)
Memory Size/Module	128 to 16K-bit	
Data Bus Width (bit)	x1 to x32 1-bit step	
Operating Voltage	3.3V, 5.0V	
Operation Frequency (Max.)	50MHz/5.0V	
Layer	3	

Series	S1X50000					
Macro Type	Standard		High-Density	High Speed		
Port	1-port	Dual port (2R+2W)	1-port	1-port	2-port (1R+1W)	Dual port (2R+2W)
Memory Size/Module	128 to 64K-bit	1K to 64K-bit	32K to 512K-bit	32K to 72K-bit		
Data Bus Width (bit)	x1 to x32 1-bit step	x8, x16, x24, x32	x8, x16, x32	x1 to x144 1-bit step		
Operating Voltage	2.0V, 2.5V, 3.0V, 3.3V		2.0V, 3.0V, 3.3V	3.3V		
Operation Frequency (Max.)	71MHz		76MHz	125MHz	110MHz	
Layer	3		3	3		

Series	S1X60000/S1K60000				
Macro Type	Standard		High-Density	High Speed	
Port	1-port	Dual port (2R+2W)	1-port	1-port	2-port (1R+1W)
Memory Size/Module	128 to 64K-bit	1K to 64K-bit	32K to 512K-bit	128 to 64K-bit	
Data Bus Width (bit)	x1 to x32 1-bit step	x8, x16, x24, x32	x8, x16, x32	x4 to x64 1-bit step	
Operating Voltage	2.0V, 2.5V			2.5V	
Operation Frequency (Max.)	125MHz	119MHz	71MHz	179MHz	
Layer	3		3	3	

Series	S1X80000/S1K80000			
Macro Type	Standard			Large Scale
Port	1-port	2-port (1R+1W)	Dual port (2R+2W)	1-port
Memory Size/Module	128 to 64K-bit	64 to 16K-bit	1K to 32K-bit	128K to 1M-bit
Data Bus Width (bit)	x1 to x32 1-bit step	x1 to x32 1-bit step	x8, x16, x24, x32	x8, x16, x32
Operating Voltage	1.8V			
Operation Frequency (Max.)	125MHz	119MHz	116MHz	74MHz
Layer	3	4	3	3

Ask our sales department regarding Gate Array SRAM.

Epson Originals -1- TCON LCD Controller ASICs

- TCON is a display control LSI with a built-in LVDS receiver, suitable for a TFT display module.
- Simply by adding or integrating various dedicated IPs such as LVDS receiver, RSDS transmitter and mini-LVDS transmitter to/with existing display timing control circuits, customers can easily develop TFT display systems in a short period of time, reduce developers' workload, and achieve a faster time to market.
- TCON IPs can be employed on a 0.35-, 0.25- or 0.15μm embedded array/standard cell, providing a developing environment equivalent to ASICs.

TCON IP Lineup

	0.35μm Series	0.25μm Series	0.18μm Series
Host interface			
6-/8-bit LVDS receiver	A	A	A
8-/10-bit LVDS receiver	—	—	A
Panel interface			
RSDS transmitter	A	A	A
mini-LVDS transmitter	—	A	A
LVDS transmitter	—	A	A
Image processing IP			
Overdrive	—	A	A
γ correction	—	A	A
Contrast correction	—	A	A
Color matrix	—	A	A
AME(Auto Movie Enhancement)	—	A	A
Others			
Spread Spectrum IP	A	A	A
Power detection circuit	A	A	A
Self oscillation circuit	—	A	A

A : Available

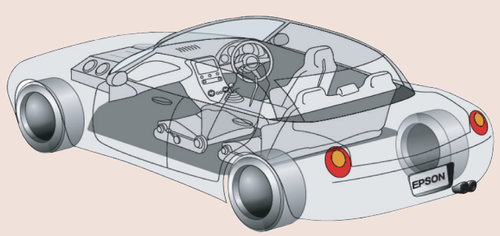
Epson Originals -2- Usable on Automobile

Achievement of ASIC on Automobile

Applications for which Epson ASICs were actually used and considered

Navigation system
Rear sheet monitor
Car audio
Instrument panels, consoles
ETC
Head-up Display

Infotainment



Body electronics

RKE, smart key
Rear view monitor
Visual aid, lane line detection
Drive Recorder
Smart Plate
Power windows and power sheets
Pressure monitoring system

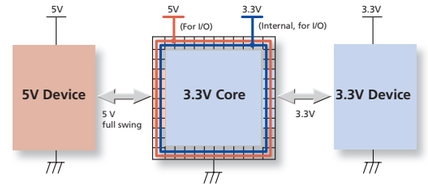
Epson Originals -3- Power System Interface

Development of low-voltage system power supplies continues as part of the trend toward reducing power consumption. However, in cases where not all system components can run on a single low-voltage power supply, multiple power supplies are used for the same system. Consequently, many of today's portable electronic devices include dual (5 V/3.3 V) power supplies, each with its own signals.

5 V/3.3 V Dual Power Supply System

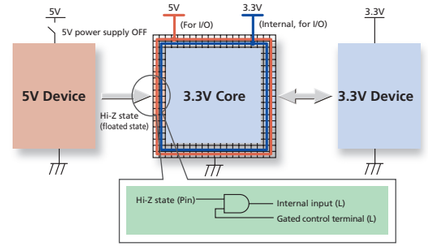
Level Shifter

Since it is often the case with ASICs that several ICs are connected in the same system, such systems are typically required to handle two types of level signals for 5 V and 3.3 V power. In S1L50000 and S1X50000 series products, the inclusion of two power supplies (such as 5 V and 3.3 V power supplies) enables the implementation of a bilevel (5 V, 3.3 V) signal interface for each I/O buffer. Such an interface is best suited for applications that include high-speed signal processing and high drive current capacity.



Gated I/O buffer

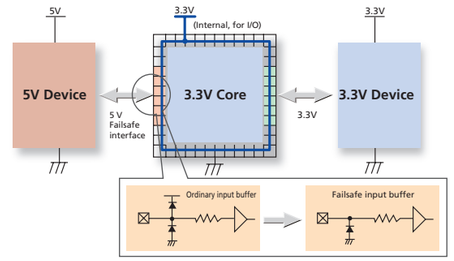
The use of the gated input buffer enables input in the Hi-Z state, which has not usually been possible using a buffer. In a system using dual-line power supply, the high-voltage power supply may be cut off. Using this function allows hot-plugging a PC card and achieving lower power consumption in the backup mode of PDA.



3.3 V Single Power Supply System

Failsafe I/O Buffer

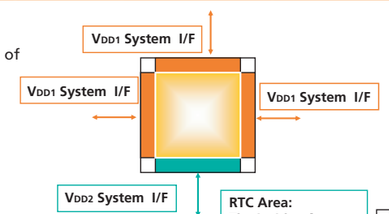
Even when system constraints preclude the implementation of a dual power supply system, it is still possible to provide an interface between a 3.3 V single power supply chip and a 5 V chip by implementing an input buffer that does not include a forward diode (in the V_{DD} direction), which also provides failsafe support for output.



Power separation suitable for low voltage power supply and low power consumption

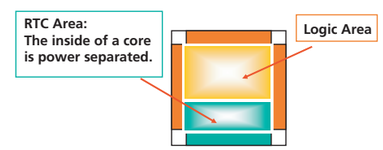
IO Power Separation

- Interface with the devices of other power systems can be possible by power separation of I/O cell area.



Core Power Separation

- When mounted with RTC, power separation between RTC area and Logic area can be possible.
  Power OFF can be possible in the non RTC area.



Epson Originals

Epson Originals -4- Countermeasures for EMI

Countermeasures for EMI

Epson ASICs will take the following countermeasures to meet requests received from many customers to reduce EMI:

- ✓ Clock gating
- ✓ Power separation
- ✓ SS (Spread Spectrum)
- ✓ Optimization of drive capacity
- ✓ Multiphase delay clock
- ✓ Optimization of PIN arrangement
- ✓ Adoption of input Schmidt circuit
- ✓ Housing of bypass condenser
- ✓ Slew rate control
- ✓ Low noise F/F

Epson Originals -5- Replacement of existing devices

For long life time applications.

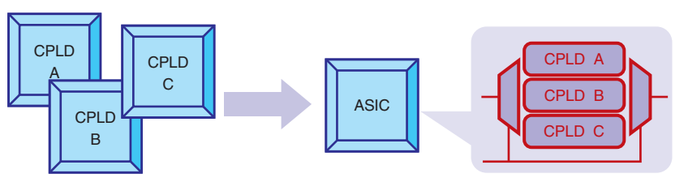
Discontinued devices

- 5V single power supply with 0.35μm process
- Pin-compatible

  Since Epson ASIC does not need fixed power pins, it is possible to replace existing devices with pin compatibility.

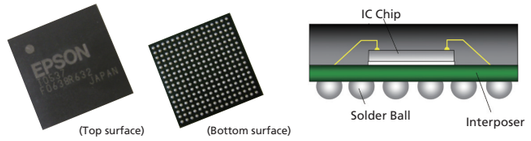
PLDs

- MP path from FPGAs or CPLDs
- Multiple CPLDs into 1 ASIC



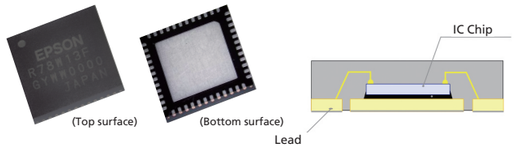
Package Lineup

Plastic Ball Grid Array (PBGA)



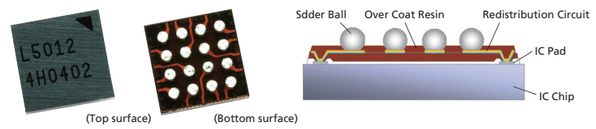
PKG Type	Body Size (mm)	Ball Pitch (mm)
PBGA1UE256 PBGA1UC256	17 X 17 X 1.7 (PBGA1UE) 17 X 17 X 1.3 (PBGA1UC)	1.0

Quad Flat Non-leaded Package (QFN)



PKG Type	Body Size (mm)	Lead Pitch (mm)
SQFN4-24	4 X 4 X 1.0	0.5
SQFN5-32	5 X 5 X 1.0	0.5
SQFN7-48	7 X 7 X 1.0	0.5
SQFN9-64	9 X 9 X 1.0	0.5

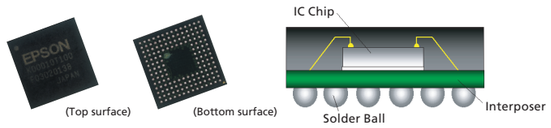
WCSP



PKG Type	Pin	Body Size (mm)	Ball Pitch (mm)
WCSP(S1L5012)	16	2.4 X 2.4 X 0.8	0.5
WCSP(S1L5028)	25	3.0 X 3.0 X 0.8	0.5
WCSP(S1L5075)	49	4.2 X 4.2 X 0.8	0.5
WCSP(S1L5125)	81	5.0 X 5.0 X 0.8	0.5
WCSP(S1L60093)	49	3.0 X 3.0 X 0.8	0.4

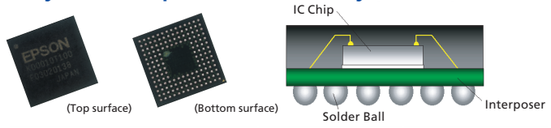
Package Externals

Plastic Fine-pitch Ball Grid Array (PFBGA)



PKG Type	Body Size (mm)	Ball Pitch (mm)
PFBGA5U-60	5 X 5 X 1.2	0.5
PFBGA5U-81	5 X 5 X 1.2	0.5
PFBGA6U-96	6 X 6 X 1.2	0.5
PFBGA6U-121	6 X 6 X 1.2	0.5
PFBGA7U-144	7 X 7 X 1.2	0.5
PFBGA7U-161	7 X 7 X 1.2	0.5
PFBGA8U-161	8 X 8 X 1.2	0.5
PFBGA8U-181	8 X 8 X 1.2	0.5
PFBGA7U-100	7 X 7 X 1.2	0.65
PFBGA8U-112	8 X 8 X 1.2	0.65
PFBGA8U-121	8 X 8 X 1.2	0.65
PFBGA10U-160	10 X 10 X 1.2	0.65
PFBGA10U-180	10 X 10 X 1.2	0.65
PFBGA12U-208	12 X 12 X 1.2	0.65
PFBGA7U-48	7 X 7 X 1.2	0.8
PFBGA8U-81	8 X 8 X 1.2	0.8
PFBGA10U-121	10 X 10 X 1.2	0.8
PFBGA10U-144	10 X 10 X 1.2	0.8
PFBGA12U-180	12 X 12 X 1.2	0.8
PFBGA14U-220	14 X 14 X 1.2	0.8
PFBGA16U-280	16 X 16 X 1.2	0.8

Very Thin Fine-pitch Ball Grid Array (VFBGA)



PKG Type	Body Size (mm)	Ball Pitch (mm)
VFBGA4H-49	4 X 4 X 1.0	0.5
VFBGA5H-81	5 X 5 X 1.0	0.5
VFBGA6H-96	6 X 6 X 1.0	0.5
VFBGA6H-121	6 X 6 X 1.0	0.5
VFBGA7H-144	7 X 7 X 1.0	0.5
VFBGA7H-161	7 X 7 X 1.0	0.5
VFBGA8H-181	8 X 8 X 1.0	0.5
VFBGA10H-240	10 X 10 X 1.0	0.5
VFBGA10H-121	10 X 10 X 1.0	0.8
VFBGA10H-144	10 X 10 X 1.0	0.8

Package Externals

ASICs

QFP & TQFP

PKG Type	Body Size (mm)	Lead Pitch (mm)
TQFP12-48	7 X 7 X 1.2	0.5
* QFP12-48	7 X 7 X 1.7	0.5
TQFP13-64	10 X 10 X 1.2	0.5
* QFP13-64	10 X 10 X 1.7	0.5
TQFP14-80	12 X 12 X 1.2	0.5
* QFP14-80	12 X 12 X 1.7	0.5
TQFP14-100	12 X 12 X 1.2	0.4
* TQFP15-100	14 X 14 X 1.2	0.5
* QFP15-100	14 X 14 X 1.7	0.5
* TQFP15-128	14 X 14 X 1.2	0.4
* QFP15-128	14 X 14 X 1.7	0.4
* QFP20-144	20 X 20 X 1.7	0.5
* QFP21-176	24 X 24 X 1.7	0.5
* QFP22-208	28 X 28 X 1.7	0.5
QFP21-216	24 X 24 X 1.7	0.4
QFP22-256	28 X 28 X 1.7	0.4

* Can be on automobile

Gate Array Package List

Epson's Gate Array Series offers various packages for each base array.
Please select the most suitable package, based on the circuit specifications and number of input/output terminals.

Gate Array Package List is subject to change due to the preparation condition of the lead frame and the improvement of production efficiency. Please consult Epson sales office when you are choosing packages.

S1L5V000 Series

AL2-Series			S1L5V012	S1L5V042	–	S1L5V112	–	S1L5V252	–	S1L5V482
AL3-Series			S1L5V013	S1L5V043	S1X5V513*	S1L5V113	S1X5V523*	S1L5V253	S1X5V533*	S1L5V483
AL4-Series			S1L5V014	S1L5V044	S1X5V514*	S1L5V114	S1X5V524*	S1L5V254	S1X5V534*	S1L5V484
Raw Gates			8.9k	42.0k	26.0k	109.3k	90.3k	254.4k	235.0k	479.9k
AL2-Usable Gates			2.7k	12.6k	–	32.8k	–	63.6k	–	119.9k
AL3-Usable Gates			5.4k	25.2k	14.3k	65.6k	49.7k	139.9k	129.3k	239.9k
AL4-Usable Gates			6.2k	29.4k	16.9k	76.5k	58.7k	165.4k	152.8k	287.9k
Pads			48	104		168		256		308
PKG	Pin	PKG Type								
TQFP	48	TQFP12-48	A	A		A				
QFP	48	QFP12-48	A	A		A				
TQFP	64	TQFP13-64		A		A		A		N
QFP	64	QFP13-64		A		A		A		N
TQFP	80	TQFP14-80		A		A				A
QFP	80	QFP14-80		A		A		A		A
TQFP	100	TQFP14-100		A		A		A		N
TQFP	100	TQFP15-100		A		A		A		LQ
QFP	100	QFP15-100		A		A		A		LQ
TQFP	128	TQFP15-128		A (104)		A		A		LQ
QFP	128	QFP15-128		A (104)		A		A		LQ
QFP	144	QFP20-144				A		A		A
QFP	176	QFP21-176	N	N		A (168)		A		LQ
QFP	208	QFP22-208	N	N		N		A		A
QFP	216	QFP21-216	N	N		N		A		LQ
QFP	256	QFP22-256	N	N		N		LQ		LQ
QFN	24	SQFN4-24	A	N		N		N		
QFN	32	SQFN5-32	A	A		N		N		
QFN	48	SQFN7-48	N	A		A		N		
QFN	64	SQFN9-64	N	A		A		A		

A: Available for mass production
LQ: Quality assurance required (Lead frame required to be developed)
N: Not available A( ): Usable up to the numbers of pins in the parenthesis
*: Analog PLL built in master

Gate Array Package List

ASICs

S1L50000 Series

AL2-Series			S1L50062	S1L50122		S1L50282	S1L50552	S1L50752	S1L50992		S1L51252	S1L51772	S1L52502	S1L53352	S1L54422	S1L55062	S1L56682	S1L58152				
AL3-Series			S1L50063	S1L50123		S1L50283	S1L50553	S1L50753	S1L50993		S1L51253	S1L51773	S1L52503	S1L53353	S1L54423	S1L55063	S1L56683	S1L58153				
AL4-Series			S1L50064	S1L50124		S1L50284	S1L50554	S1L50754	S1L50994		S1L51254	S1L51774	S1L52504	S1L53354	S1L54424	S1L55064	S1L56684	S1L58154				
Raw Gates			5.8k	12.0k		28.8k	55.5k	75.8k	99.2k		125.8k	177.1k	250.2k	335.9k	442.2k	506.7k	668.6k	815.5k				
AL2-Usable Gates			2.9k	6.0k		14.4k	26.1k	35.7k	46.7k		56.6k	79.7k	112.6k	144.5k	176.9k	202.7k	267.5k	326.2k				
AL3-Usable Gates			5.1k	10.6k		25.3k	47.2k	64.4k	84.4k		100.7k	132.8k	187.7k	251.9k	309.5k	354.7k	468.0k	570.9k				
AL4-Usable Gates			5.5k	11.4k		27.3k	52.8k	72.0k	94.3k		119.5k	168.2k	237.7k	319.1k	397.9k	456.1k	601.7k	734.0k				
Pads			48	64	56	104	88	144	124	168	144	192	168	216	188	224	264	308	352	376	432	480
Pad Pitch			70μ	70μ	80μ	70μ	80μ	70μ	80μ	70μ	80μ	70μ	80μ	70μ	80μ	80μ	80μ	80μ	80μ	80μ	80μ	80μ
PKG	Pin	PKG Type																				
TQFP	48	TQFP12-48	A	A	A		A	A	A		A		N									
QFP	48	QFP12-48	A	A	A		A	A	A		A		A	N								
TQFP	64	TQFP13-64		A	A		A	A	A		A		A	A	LQ	N	N					
QFP	64	QFP13-64		A	A(56)		A	A	A		A		A	A	A	N	N					
TQFP	80	TQFP14-80	A	A	A	A	A	A	A		A		A	A	A	A						
QFP	80	QFP14-80	A	A	A	A	A	A	A		A		A	A	A	A	N					
TQFP	100	TQFP15-100				A	A(88)	A	A		A		A		A	LQ	A	LQ	LQ	N	N	
QFP	100	QFP15-100				A	A(88)	A	A		A		A		A	A	A	LQ	LQ	N	N	
TQFP	128	TQFP15-128				A(104)		A			A		A		A	A	A	LQ	LQ	N	N	
QFP	128	QFP15-128				A(104)		A			A		A		A	A	A	LQ	LQ	N	N	
QFP	144	QFP20-144					LQ	A			A		A		A	A	A	A	LQ	LQ	LQ	N
QFP	176	QFP21-176	N	N	N	N	N	N		A(168)		A	A(168)		A	A	A	LQ	LQ			
QFP	208	QFP22-208	N	N	N	N	N	N		N		N	N	N	N	A	A	A	A	N	N	N
QFP	216	QFP21-216	N	N	N	N	N	N		N	N	N	N	A	A	A	LQ	LQ	LQ	N	N	N
QFP	256	QFP22-256	N	N	N	N	N	N		N	N	N	N	N	N	N	LQ	LQ	LQ	A	A	N
QFN	24	SQFN4-24	A	A	A	N	N															
QFN	32	SQFN5-32	A	A	A		A		N													
QFN	48	SQFN7-48	A	A	A		A		A		A		A		A							
QFN	64	SQFN9-64		A	A(56)		A		A		A		A		A	A	A					

A: Available for mass production
LQ: Quality assurance required (Lead frame required to be developed)
N: Not available A( ): Usable up to the numbers of pins in the parenthesis

Gate Array Package List

S1L60000 Series

		AL3-Series	S1L60093	S1L60173	S1L60283	S1L60403	S1L60593	S1L60833	S1L61233	S1L61583	S1L61903	S1L62513
		AL4-Series	S1L60094	S1L60174	S1L60284	S1L60404	S1L60594	S1L60834	S1L61234	S1L61584	S1L61904	S1L62514
		Raw Gates	99.2k	171.8k	284.4k	400.3k	595.4k	831.6k	1,234.9k	1,587.8k	1,903.0k	2,519.6k
		AL3-Usable Gates	59.6k	103.1k	142.2k	200.2k	297.7k	332.7k	494.0k	635.1k	761.2k	1,007.9k
		AL4-Usable Gates	69.5k	120.2k	184.9k	260.2k	387.0k	415.8k	617.5k	793.9k	951.5k	1,259.8k
		70μm Pads	112	148	188	224	272	-	-	-	-	-
		80μm Pads	-	-	-	-	-	284	344	388	424	488
PKG	Pin	PKG Type										
TQFP	48	TQFP12-48	A	A	A	N						
QFP	48	QFP12-48	A	A	A	N						
TQFP	64	TQFP13-64	A	A	A	A	A	LQ				
QFP	64	QFP13-64	A	A	A	A	A	A				
TQFP	80	TQFP14-80	A	A	A	A	A	A	A			
QFP	80	QFP14-80	A	A	A	A	A	A	A			
TQFP	100	TQFP14-100	A	A	A	A	A	N				
TQFP	100	TQFP15-100	A	A	A	A	A	LQ	LQ			
TQFP	128	TQFP15-128	A	A	A	A	A	LQ	LQ	N		
QFP	128	QFP15-128	A	A	A	A	A	LQ	LQ	N		
QFP	144	QFP20-144	N	A	A	A	A	A	LQ	LQ	N	
QFP	176	QFP21-176	N	N	A	A	A	A	LQ	N	N	
QFP	208	QFP22-208	N	N	LQ	LQ	A	A	A	N		
QFP	216	QFP21-216	N	N	N	A	A	LQ	LQ	N	N	N
QFP	256	QFP22-256	N	N	N	N	LQ	LQ	LQ	LQ	LQ	N
QFN	24	SQFN4-24	N	N	N							
QFN	32	SQFN5-32	A	N	N							
QFN	48	SQFN7-48	A	A	A	A						
QFN	64	SQFN9-64	A	A	A	A	A	A	N			

A: Available for mass production
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N: Not available A( ): Usable up to the numbers of pins in the parenthesis

Package's Thermal Resistance

ASICs

Among LSIs, chip temperatures (T_j) rise as power consumption increases. The chip temperature of a packaged IC can be calculated based on the ambient temperature T_a, the package's thermal resistance $\theta_{j\text{-}a}$, and the power dissipation P_D as shown below.

Chip temperature (T_j) = T_a + (P_D x $\theta_{j\text{-}a}$) (˚C)

As a general rule, the chip temperature (T_j) should be kept under 125˚C. Note also that the package's thermal resistance varies widely depending on the mounting method and the presence or absence of forced cooling.

QFP

Package Type	$\theta_{j\text{-}a}$ (℃／W)			$\theta_{j\text{-}c}$
	0m/sec	1m/sec	2m/sec	(℃／W)
QFP12	51	46	44	6
QFP13	48	45	43	6
QFP14	44	41	39	6
QFP15	41	39	37	6
QFP20	36	33	31	6
QFP21	34	31	29	6
QFP22	27	24	23	6
TQFP12	53	47	45	4
TQFP13	47	44	42	4
TQFP14	43	40	38	4
TQFP15	42	36	34	4

SQFN

Package Type	$\theta_{j\text{-}a}$ (℃／W)			$\theta_{j\text{-}c}$
	0m/sec	1m/sec	2m/sec	(℃／W)
SQFN4	42	39	37	5
SQFN5	40	37	35	5
SQFN7	31	28	25	5
SQFN9	26	23	21	5

PBGA

Package Type	$\theta_{j\text{-}a}$ (℃／W)			$\theta_{j\text{-}c}$
	0m/sec	1m/sec	2m/sec	(℃／W)
PBGA1U	24	21	20	4

PFBGA

Package Type	$\theta_{j\text{-}a}$ (℃／W)			$\theta_{j\text{-}c}$
	0m/sec	1m/sec	2m/sec	(℃／W)
PFBGA5	43	40	38	3
PFBGA6	40	37	35	3
PFBGA7	34	31	30	3
PFBGA8	31	28	27	3
PFBGA10	30	22	21	3
PFBGA12	24	21	20	3
PFBGA13	23	21	20	3
PFBGA14	22	20	19	3
PFBGA16	20	18	17	3

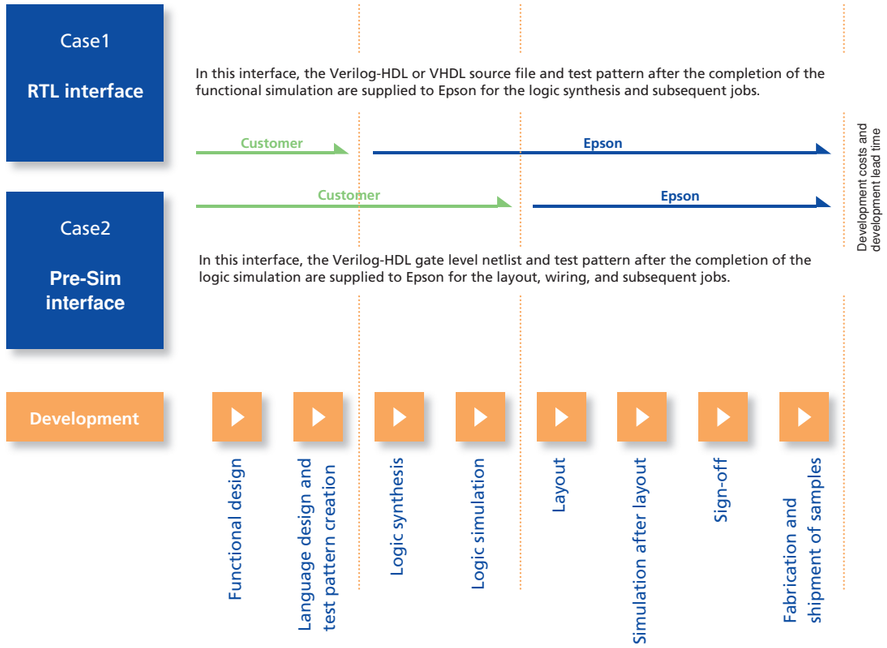
VFBGA

Package Type	$\theta_{j\text{-}a}$ (℃／W)			$\theta_{j\text{-}c}$
	0m/sec	1m/sec	2m/sec	(℃／W)
VFBGA4	48	45	43	3
VFBGA5	43	40	38	3
VFBGA6	40	37	35	3
VFBGA7	34	31	30	3
VFBGA8	31	28	27	3
VFBGA10	30	22	21	3

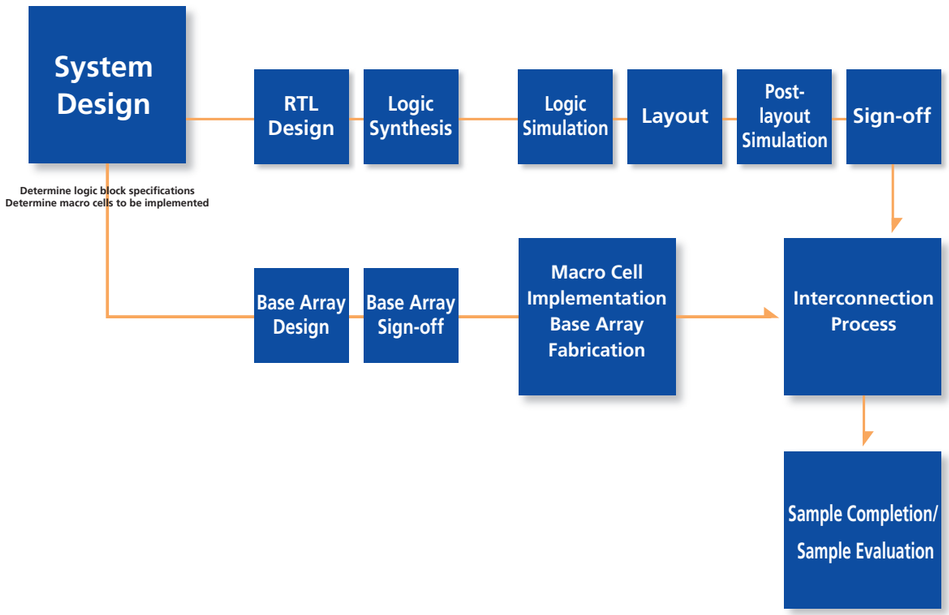
- Values listed above are typical values, but the thermal resistance can easily vary depending on conditions. Allow the margin of Max. ±15°C/W at θj-a and Max. ±3°C/W at θj-c
- QFP, QFN, PBGA
  Implementation board: JEDEC standard board
  (114.3 x 76.2 x 1.6mm, 4 layers)
- PFBGA, VFBGA
  Implementation board: (114.5 x 101.5 x 1.6mm, 4 layers)
- Values listed above are shown only for reference, as they are not guantitative values.

User Interface

In order to flexibly comply with the customer's design stages, Epson offers two types of user interfaces. The development lead time and development costs are determined by the interface of your choice.

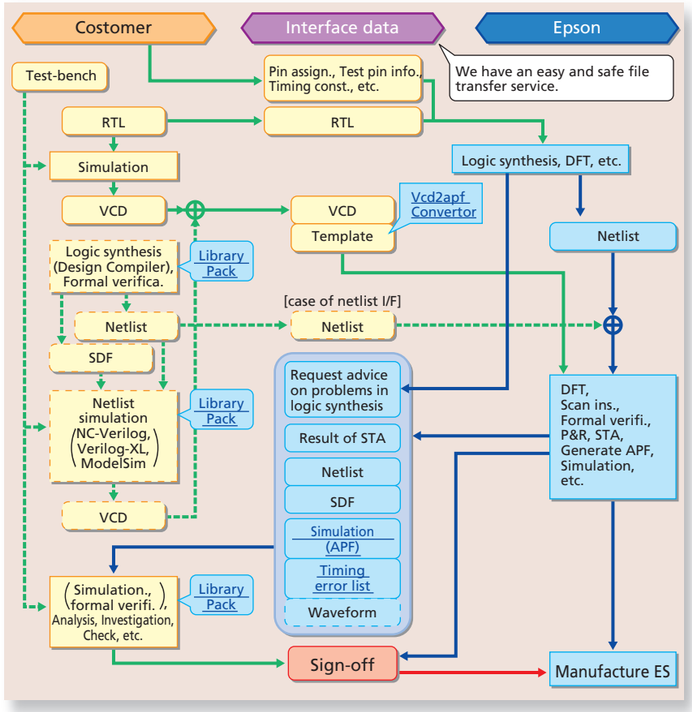


Design of Embedded Array Chips



Development Flow

Interface Flow



Library Pack

Supported series

Technology	0.35µm	0.25µm	0.15µm
Gate Array	S1L50000 S1L5V000	S1L60000	-
Embedded Array	S1X5V000 S1X50000	S1X60000	(S1X80000)
Standard cell	-	S1K60000	S1K80000

Supported tools

Category	Tool name
Logic synthesizer	Design Compiler
Simulator	Verilog-XL, NC-Verilog, ModelSim(Verilog), ModelSim(VHDL)*

* : Not available for S1L5V000, S1X5V000, S1X80000, S1K80000 series

Epson ASIC Website

■Epson Website Presents ASIC product information

<global.epson.com/products_and_drivers/semicon/products/asic/>

<ASIC HP>